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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/708,236

02/18/2004

Miles G. Canada

BUR920040014US1

2235

30449

7590

08/01/2005

SCHMEISER, OLSEN + WATTS

3 LEAR JET LANE

SUITE 201

LATHAM, NY 12110

EXAMINER

LE, THONG QUOC

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

JK

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/708,236		CANADA ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Thong Q. Le		2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-7,9 and 11-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-7,9 and 11-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. ____   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____  | 6) <input type="checkbox"/> Other: ____                                     |

### **DETAILED ACTION**

1. Amendment filed on 05/31/2005 has been entered.
2. Claims 1,8,10 have been canceled.
3. Claims 2-7, 9,11-21 are presented for examination.

### ***Response to Arguments***

4. Applicant's arguments, see amendment, filed 05/31/2005, with respect to 1-9,11-21 have been fully considered and are persuasive. The rejection of previous action has been withdrawn.

### ***Claim Objections***

5. Regarding claims 2, 9, line 6, should be changed "said memory array" to –said memory cell array—as defined in line 2.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 2-7,9,11-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Guddat et al. (U.S. Patent No. 6,366,99).

Regarding claims 2-7,9,11-21, Guddat et al. disclose an electronic circuit (Figure 1), comprising:

a memory cell array (106); a sense amplifier self-timed decode circuit (172, 116, 139) adapted to set a base read time delay of the memory cell array (Column 8, lines 53-65, Column 9, lines 16-29, Column ); a read delay adjustment circuit (Column 3, lines 40-61, Column 9, lines 29-50) coupled to the memory cell array, the read delay adjustment circuit adapted to adjust the based read time delay of the memory cell array based on an operating frequency of the memory cell array; a sense amplifier delay circuit (139, 151) Column coupled between the sense amplifier self-timed decode circuit and the memory cell array, the sense amplifier delay circuit adapted to the control an amount of the delay time added to the base read time delay in response to a margin select signal (Column 29-67, Column 10, lines 1-60); and a read margin adjustment circuit (Column 9, lines 37-67, Column 10, lines 1-8) coupled to the sense amplifier delay circuit, the read margin adjustment circuit adapted to generate the margin select signal, and a microprocessor (Column 1, lines 11-40, Column 3, lines 12-32) adapted to execute a load instruction issued in response to a change of value of the operating frequency of the microprocessor and of the memory cell array and to store data associated with the load instruction in a register, an output of the register coupled to the sense amplifier delay circuit (Column 4, lines 14-48), and wherein the read margin circuit includes a frequency selection circuit adapted the operating frequency of the memory cell array from internal generation circuit or from external clock signal, and frequency detector coupled between the frequency selection circuit and the sense amplifier delay circuit (Column 3, lines 40-55), and including one or more programmable fuses (Figure 1, 139) coupled to the sense amplifier delay circuit, the sense amplifier

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adapted to set an initial time adjustment to the base read time delay based on a state of one or more fuses (Column 3, lines 55-67, Column 4, lines 1-22), and the sense amplifier delay circuit is adapted to override the initial time adjustment based on the margin select signal (Column 4, lines 14-22), and when the operating frequency is to be decreased, sequentially decreasing the operating frequency, issuing the margin select signal and decreasing the operating voltage in the order recited and when the operating frequency is to be increased, sequentially increasing the operating voltage, issuing the margin select signal and increasing the operating voltage in the order recited (Column 11, lines 18-48).

Regarding claims 11, 21, the apparatus discussed above would perform the method claims 11,21.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le  
Primary Examiner  
Art Unit 2827

**THONG LE**  
**PRIMARY EXAMINER**